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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/813,530	03/29/2004	Volker Harle	P2001,0678	5329

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EXAMINER	
LUU, CHUONG A	
ART UNIT	PAPER NUMBER
2818	

DATE MAILED: 08/23/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/813,530	HARLE ET AL.	
	Examiner	Art Unit	
	Chuong A. Luu	2818	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 6/12/2006.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-25 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-25 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

Applicant's arguments with respect to claims 1-25 have been considered but are moot in view of the new ground(s) of rejection.

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

The Rejections

Claims 1 and 3-7 are rejected under 35 U.S.C. 102(e) as being anticipated by Chong et al. (U.S. 2002/0045355 A1).

Chong discloses a method for manufacturing a semiconductor device with

(1) providing a semiconductor body containing a substrate (120) and at least one nitride compound semiconductor disposed (122) on the substrate (120) (see Figure 6);

applying a metal layer to a surface of the semiconductor body (see Figure 22);

dry-chemically removing a part of the metal layer and a part of the emiconductor body previously covered by the removed metal layer (see paragraphs [0067]-[0068]. Figures 6-8);

(3) wherein the dry-chemically removing step is preformed by the steps of: forming a mask on the metal layer, a part of the metal layer not being covered by the mask (see paragraph [0068]);

removing that part of the metal layer which is not covered by the mask, a part of the surface of the semiconductor body thereby being uncovered and defining an uncovered surface;

partially removing the semiconductor body in regions of the uncovered surface; and removing the mask (see paragraphs [0067]-[0068]. Figures 6-8);

(4) which further comprises forming the mask as a dielectric mask which contains at least one material selected from the group consisting of silicon oxide (see paragraphs [0050]);

(5) which further comprises fabricating the mask photolithographically, in which a photoresist mask is fabricated on the mask (see paragraphs [0067]-[0068]);

(6) which further comprises removing the metal layer by a sputtering-back method (see paragraphs [0067]-[0068]);

(7) which further comprises removing the part of the semiconductor body by an etching method (see paragraphs [0067]-[0068]).

PRIOR ART REJECTIONS

Statutory Basis

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The Rejections

Claims 8-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong et al. (U.S. 2002/0045355 A1) in view of Iguchi (U.S. 2002/0076936 A1).

Chong teaches the above outlined features except for applying a passivation layer to the surface of the semiconductor body and part of the metal layer, at least a further part of the metal layer not being covered by the passivation layer. However, Iguchi discloses a semiconductor device with **(8)** which further comprises applying a passivation layer to the surface of the semiconductor body and part of the metal layer, at least a further part of the metal layer not being covered by the passivation layer (see Figure 25); **(9)** wherein the step of applying the passivation layer further comprises the steps of: applying the passivation layer as a continuous passivation layer to the surface of the semiconductor body and the part of the metal layer; applying a mask on the continuous passivation layer, the mask not covering the passivation layer at least in a region in which the passivation layer adjoins the metal layer; removing parts of the

passivation layer which are not covered with the mask; and removing the mask (see Figures 25-26); **(10)** which further comprises forming the passivation layer to contain a silicon oxide (see see paragraph [0190]. Figure 26); **(11)** which further comprises fabricating the mask photolithographically (see Figures 25-26); **(12)** which further comprises applying a contact metallization (see Figure 26). Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify of Chong's devices (in accordance with the teaching Iguchi). Doing so would facilitate the manufacture of the semiconductor device and enhance the performance of the semiconductor device.

Claims 2 and 14-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Chong et al. (U.S. 2002/0045355 A1) in view of Ota et al. (U.S. 6,335,218 B1) and further in view of Shibata et al. (U.S. 6,008,539).

Chong teaches everything above except for forming the nitride compound semiconductor as a compound having a formula $Al_yIn_xGa_{1-x-y}N$, $0<x<1$, $0<y<1$, $0<x+y<1$; the thickness of metal layer; selecting platinum and palladium as metal materials.

However, Ota discloses a semiconductor device with **(2)** which further comprises forming the nitride compound semiconductor as a compound having a formula $Al_yIn_xGa_{1-x-y}N$, $0<x<1$, $0<y<1$, $0<x+y<1$ (see column 4, lines 25-30); **(14)** which further comprises forming a thickness of the metal layer to be 200 nm (between 5 nm and 500 nm) (see column 7, lines 47-48); **(15)** which further comprises forming the semiconductor body to be p-doped in a region adjoining the metal layer (see column 5,

lines 25-55 and column 6, lines 23-38); **(16)** which further comprises doping the p-doped region of the semiconductor body with a material selected from the group consisting of magnesium and ZinC (see column 5, lines 25-55 and column 6, lines 23-38); **(17)** which further comprises forming the semiconductor body with a radiation-generating active layer; **(18)** wherein a semiconductor ridge structure is shaped by the partially removing of the semiconductor body step (see Figure 6); **(19)** wherein the semiconductor ridge structure forms a waveguide at least for parts of radiation generated by the active layer; **(20)** wherein the semiconductor component a luminescence diode (see column 3, lines 1-2); **(21)** wherein the luminescence diode is selected from the group consisting of light-emitting diodes, laser diodes, and laser diodes with a ridge waveguide (see column 3, lines 1-17); **(22)** which further comprises forming the substrate to be n-conducting (see column 5, lines 25-55 and column 6, lines 23-38); **(23)** which further comprises forming the substrate to be selected from the group consisting of n-doped SiC and n-doped GaN (see column 5, lines 25-55 and column 6, lines 23-38); **(24)** which further comprises forming a thickness of the metal layer to be 200 nm (between 40 nm and 120 nm) (see column 7, lines 47-48); **(25)** which further comprises removing the metal layer by an etching method (see column 7, lines 51-52).

Furthermore, Shibata discloses a semiconductor with **(13)** which further comprises forming the metal layer to contain a material selected from the group consisting of platinum and palladium (see column 5, lines 52-59). It would have been obvious to one having ordinary skill in the art at the time the invention was made to

modify of Chong and Ota's devices (in accordance with the teaching Shibata) and it also has been held that where the general conditions of a claim are disclosed in the prior ad, discovering the optimum or workable ranges involves only routine skill in the art and it is noted that the applicant does not disclose criticality in the ranges claimed. In re Aller, 105 USPQ 233 (see MPEP 2144.05). Also, since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice. In re Leshin, 125 USPQ 416. Doing so would facilitate the manufacture of the semiconductor device and increase the speed of the semiconductor structure.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chuong A. Luu whose telephone number is (571) 272-1902. The examiner can normally be reached on M-F (6:15-2:45).

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Smith can be reached on (571) 272-1907. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chuong Anh Luu
Patent Examiner
August 08, 2006